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10CS74

Seventh Semester B.E. Degree Examination, June/July 2018
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Define computer architecture. Illustrate the seven dimensions of an ISA. **(08 Marks)**

b. Find the die yield for dies that are 1.5 cm on a side and 1.0 cm on a side, assuming the wafer yield is 100%, defect density of 0.4 per cm^2 and α is 4. **(06 Marks)**

c. Briefly explain quantitative principles of computer design. **(06 Marks)**

2 a. List pipeline hazards. Explain structural hazard in detail. **(08 Marks)**

b. An unpipelined processor has 1 ns clock cycle and it uses 4 cycles for ALU operation and branches, 5 cycles for memory operations. Assume that relative frequencies of these operations are 40%, 20% and 40% respectively. Suppose due to clock skew and setup, pipelining the processor adds 0.2 ns of overhead to the clock. Find the speed up from pipelining by ignoring latency impact. **(05 Marks)**

c. List and explain five semi independent ways of classifying exceptions in a computer system. **(07 Marks)**

3 a. Explain true data dependences, name dependences and control dependence with necessary code segment. **(06 Marks)**

b. Show how the below MIPS straight forward code looks on MIPS 5 stage pipeline under the following situations. Find the number of clock cycles per iterations, for each case. Assume the latencies for integer and floating point operations as given in prescribed text book.

```
Loop : L.D   F0, 0(R1)
       ADD. D  F4, F0, F2
       S.D   F4, 0(R1)
       DADDUI   R1, R1, #-8
       BNE   R1, R2, Loop
```

i) Without scheduling and without loop unrolling
ii) With scheduling and without loop unrolling
iii) With loop unrolling 4 times and without scheduling
iv) With loop unrolling 4 times and with scheduling **(08 Marks)**

c. Explain Tomasulo's algorithm with basic structure of MIPS floating point unit. **(06 Marks)**

4 a. Explain briefly the basic VLIW approach and also the problems that make the approach less efficient. **(08 Marks)**

b. With a neat diagram explain the steps involved in handling an instruction with a branch target buffer. Also evaluate how well it works. **(08 Marks)**

c. Write a note on value prediction. **(04 Marks)**

PART – B

5 a. Explain the different taxonomy of parallel architecture. **(06 Marks)**

b. What is multiprocessor cache coherence? Explain snooping based cache coherence along with state transition diagram. **(10 Marks)**

c. How a single atomic memory operation is implemented for memory read and write in a single, uninterruptible instruction? **(04 Marks)**

6 a. Explain four memory hierarchy questions in detail. **(08 Marks)**

b. With a diagram, explain the organization of data cache in the opetron microprocessor. **(06 Marks)**

c. Assume we have a computer where the CPI is 1.0 when all memory accesses hit in the cache. The only data accesses are loads and stores, and these total 50% of the instructions. If the miss penalty is 25 clock cycles and the miss rate is 2%, how much faster would the computer be if all instructions were cache hits? **(06 Marks)**

7 a. List and explain three C's model that sorts all cache misses. **(06 Marks)**

b. List advanced cache optimization and explain any three optimization methods in detail. **(10 Marks)**

c. Briefly explain how memory protection is enforced via virtual memory. **(04 Marks)**

8 a. Explain in detail the hardware support for preserving exception behavior during speculation. **(10 Marks)**

b. Explain the IA 64 register model, instruction set and also the prediction and speculation support provided. **(10 Marks)**

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